

SN54ALS996, SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

SDAS098B – OCTOBER 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/\bar{C} Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable (\bar{EN}) input is low. Data can be read back onto the data inputs by taking the read (\bar{RD}) input low, in addition to having \bar{EN} low. When \bar{EN} is high, both the read-back and write modes are disabled. Transitions on \bar{EN} should only be made with CLK high to prevent false clocking.

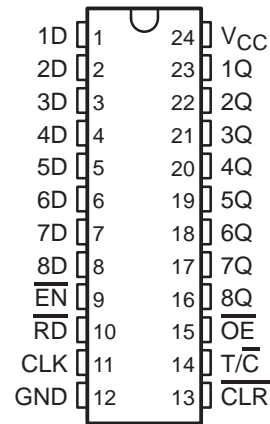
The polarity of the Q outputs can be controlled by the polarity (T/\bar{C}) input. When T/\bar{C} is high, Q is the same as is stored in the flip-flops. When T/\bar{C} is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable (\bar{OE}) input high. \bar{OE} does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear (\bar{CLR}) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

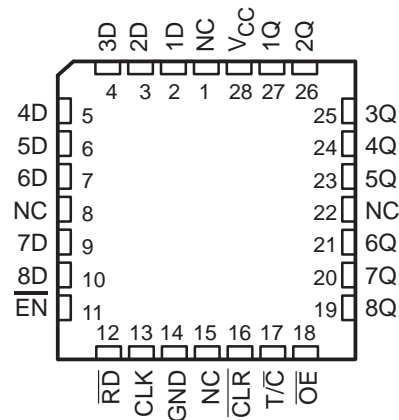
The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

The SN54ALS996 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS996 is characterized for operation from 0°C to 70°C .

SN54ALS996 . . . JT PACKAGE
SN74ALS996 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS996 . . . FK PACKAGE
(TOP VIEW)



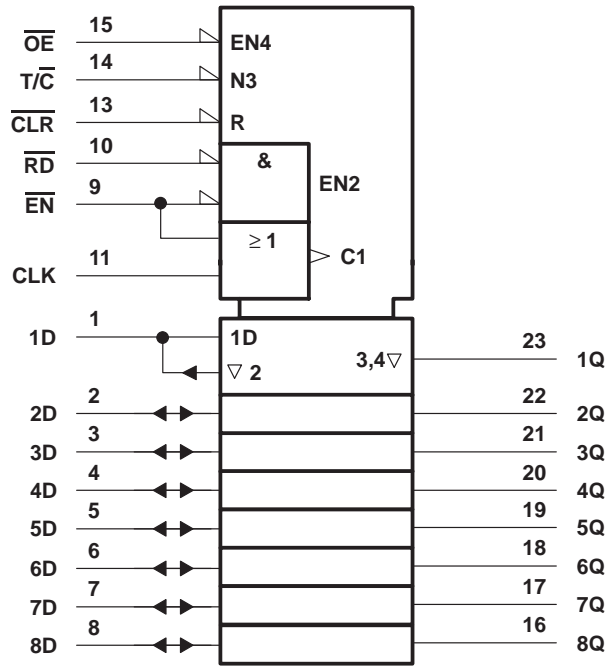
NC – No internal connection

SN54ALS996, SN74ALS996

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

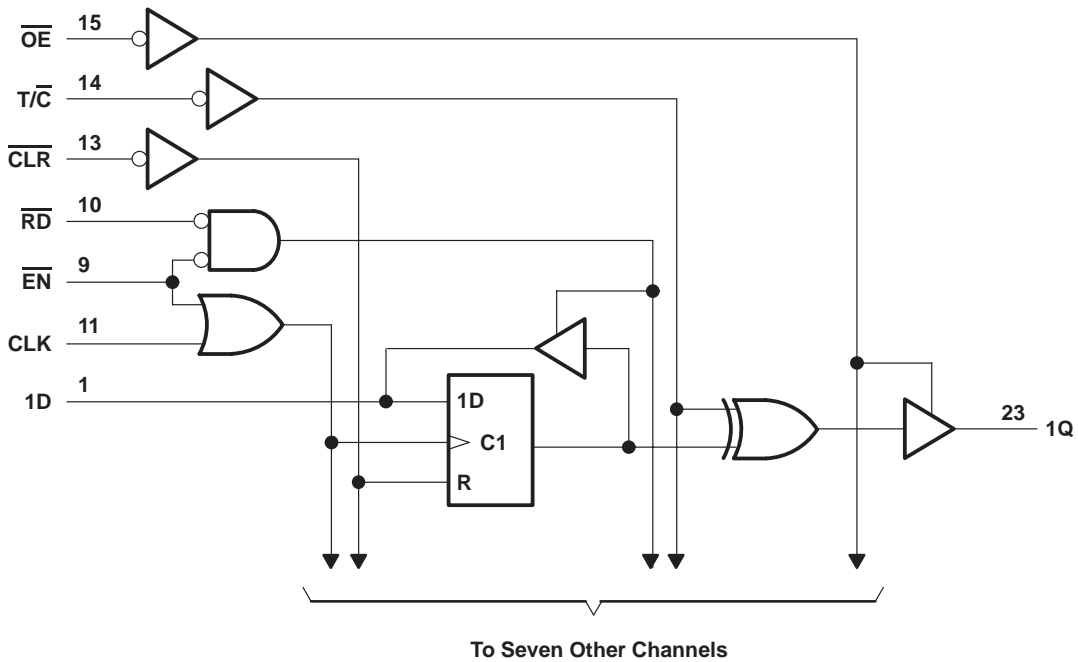
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)

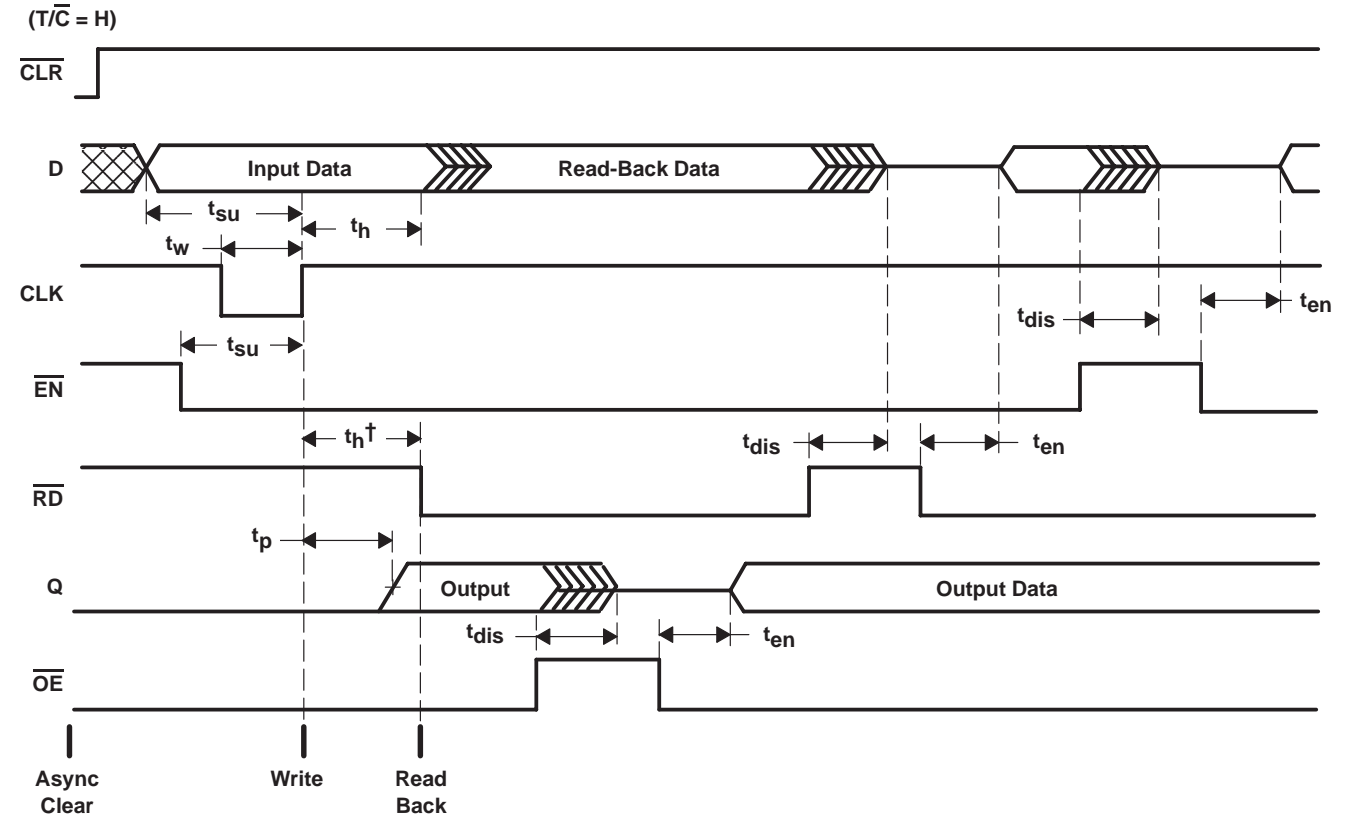


Pin numbers shown are for the DW, JT, and NT packages.

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timing diagram



† This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I (\overline{OE} , \overline{RD} , \overline{EN} , CLK, \overline{CLR} , and T/\overline{C}) | 7 V |
| Voltage applied to D inputs and to disabled 3-state outputs | 5.5 V |
| Operating free-air temperature range, T_A : SN54ALS996 | -55°C to 125°C |
| SN74ALS996 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

| | | SN54ALS996 | | | SN74ALS996 | | | UNIT |
|--------------------|--------------------------------|---|-----|-----|------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | All inputs | | | 2 | | | V |
| | | All inputs except \overline{OE} , \overline{RD} | | | 2 | | | |
| | | \overline{OE} , \overline{RD} | | | 2.2 | | | |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | Q | | | -1 | | | mA |
| | | D | | | -0.4 | | | |
| I _{OL} | Low-level output current | Q | | | 12 | | | mA |
| | | | | | 24 | | | |
| | | D | | | 8 | | | |
| f _{clock} | Clock frequency | 0 | | 35 | 0 | | 35 | MHZ |
| t _w | Pulse duration | \overline{CLR} low | | | 10 | | | ns |
| | | CLK low | | | 14.5 | | | |
| | | CLK high | | | 14.5 | | | |
| t _{su} | Setup time | Data before CLK↑ | | | 15 | | | ns |
| | | \overline{EN} low before CLK↑ | | | 10 | | | |
| | | CLK high before \overline{EN} ↑‡ | | | 15 | | | |
| | | \overline{CLR} high (inactive) before CLK↑ | | | 10 | | | |
| t _h | Hold time | Data after CLK↑ | | | 1 | | | ns |
| | | \overline{EN} low after CLK↑ | | | 5 | | | |
| | | \overline{RD} high after CLK↑§ | | | 5 | | | |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

† Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V

‡ This setup time ensures that \overline{EN} will not false clock the data register.

§ This hold time ensures that there will be no conflict on the input data bus.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS996 | | SN74ALS996 | | UNIT | |
|------------------|-------------------------------------|---|------------------|--------------------------|----------|---------------------|----------|------|------|
| | | | | MIN | TYP† | MAX | MIN | | TYP† |
| V _{IK} | | V _{CC} = 4.5 V, I _I = -18 mA | | -1.2 | | -1.2 | | V | |
| V _{OH} | All outputs | V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA | | V _{CC} - 2 | | V _{CC} - 2 | | V | |
| | Q | V _{CC} = 4.5 V | | 2.4 | 3.2 | | | | |
| V _{OL} | D | V _{CC} = 4.5 V | | I _{OL} = 4 mA | | 0.25 0.4 | | V | |
| | | | | I _{OL} = 8 mA | | | | | |
| | Q | V _{CC} = 4.5 V | | I _{OL} = 12 mA | | 0.25 0.4 | | | |
| | | | | I _{OL} = 24 mA | | 0.35 0.5 | | | |
| | | | | I _{OL} = 48 mA‡ | | 0.35 0.5 | | | |
| I _{OZH} | Q | V _{CC} = 5.5 V, V _O = 2.7 V | | 20 | | 20 | | μA | |
| I _{OZL} | Q | V _{CC} = 5.5 V, V _O = 0.4 V | | -20 | | -20 | | μA | |
| I _I | D inputs | V _{CC} = 5.5 V | | V _I = 5.5 V | | 0.1 | | mA | |
| | All others | | | V _I = 7 V | | 0.1 | | | |
| I _{IH} | D inputs§ | V _{CC} = 5.5 V, V _I = 2.7 V | | 20 | | 20 | | μA | |
| | All others | | | 20 | | 20 | | | |
| I _{IL} | D inputs§ | V _{CC} = 5.5 V, V _I = 0.4 V | | -0.1 | | -0.1 | | mA | |
| | All others | | | -0.1 | | -0.1 | | | |
| I _O ¶ | | V _{CC} = 5.5 V, CLR = 2.5 V | | -20 -112 | | -30 -112 | | mA | |
| I _{CC} | V _{CC} = 5.5 V, EN, RD low | | Outputs high | | 35 55 | | 35 55 | | mA |
| | | | Outputs low | | 55 85 | | 55 85 | | |
| | | | Outputs disabled | | 42 65 | | 42 65 | | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V

§ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 1)

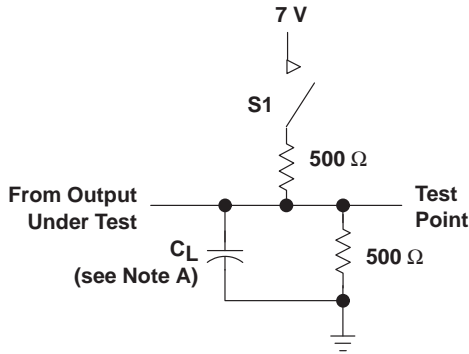
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX† | | | | UNIT |
|--------------------|------------------------|----------------|--|-----|------------|-----|------|
| | | | SN54ALS996 | | SN74ALS996 | | |
| | | | MIN | MAX | MIN | MAX | |
| f _{max} | | | 35 | | 35 | MHz | |
| t _{PLH} | CLK (T/C̄ = H or L) | Q | 5 | 30 | 5 | 28 | ns |
| t _{PHL} | | | 5 | 24 | 5 | 28 | |
| t _{PLH} | CLR (T/C̄ = L) | Q | 5 | 27 | 7 | 27 | ns |
| t _{PHL} | | | CLR (T/C̄ = H) | 5 | 23 | 7 | |
| t _{PLH} | T/C̄ | Q | 4 | 23 | 5 | 23 | ns |
| t _{PHL} | | | 5 | 23 | 5 | 23 | |
| t _{PHL} | CLR | D | 5 | 30 | 8 | 30 | ns |
| t _{en} ‡ | RD | D | 2 | 18 | 3 | 16 | ns |
| t _{dis} § | | | 1 | 19 | 3 | 19 | |
| t _{en} ‡ | EN | D | 2 | 17 | 3 | 16 | ns |
| t _{dis} § | | | 1 | 19 | 3 | 19 | |
| t _{en} ‡ | OE | Q | 2 | 15 | 4 | 15 | ns |
| t _{dis} § | | | 1 | 11 | 1 | 10 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

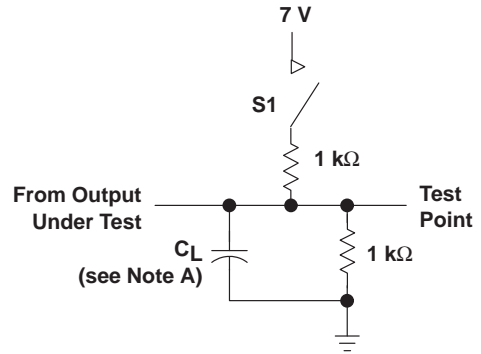
‡ t_{en} = t_{PZH} or t_{PZL}

§ t_{dis} = t_{PHZ} or t_{PLZ}

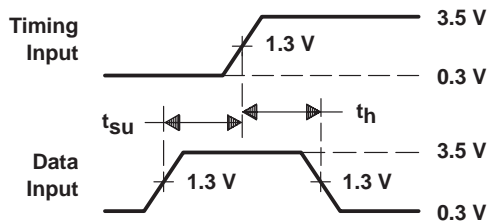
PARAMETER MEASUREMENT INFORMATION



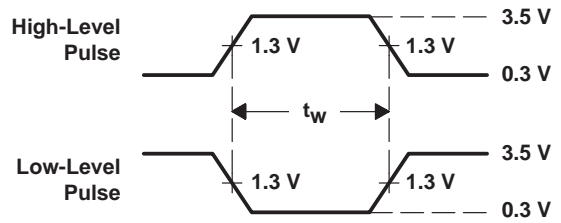
LOAD CIRCUIT FOR Q OUTPUTS



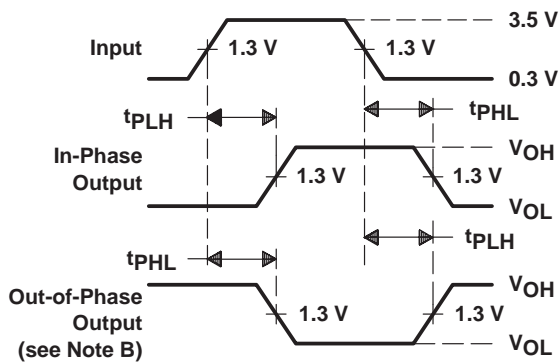
LOAD CIRCUIT FOR D OUTPUTS



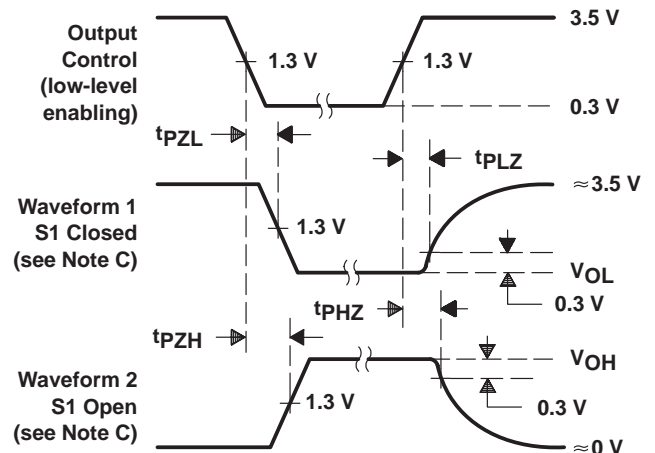
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

B. When measuring propagation delay times of 3-state outputs, switch S1 is open.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-89945013A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-89945014A | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74ALS996-1DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996-1DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996-1DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996-1DWR | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI |
| SN74ALS996-1NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS996-1NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS996DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS996NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS996NT3 | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI |
| SN74ALS996NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SNJ54ALS996FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ALS996JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54ALS996W | OBSOLETE | CFP | W | 24 | | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS996DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS996DWR | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



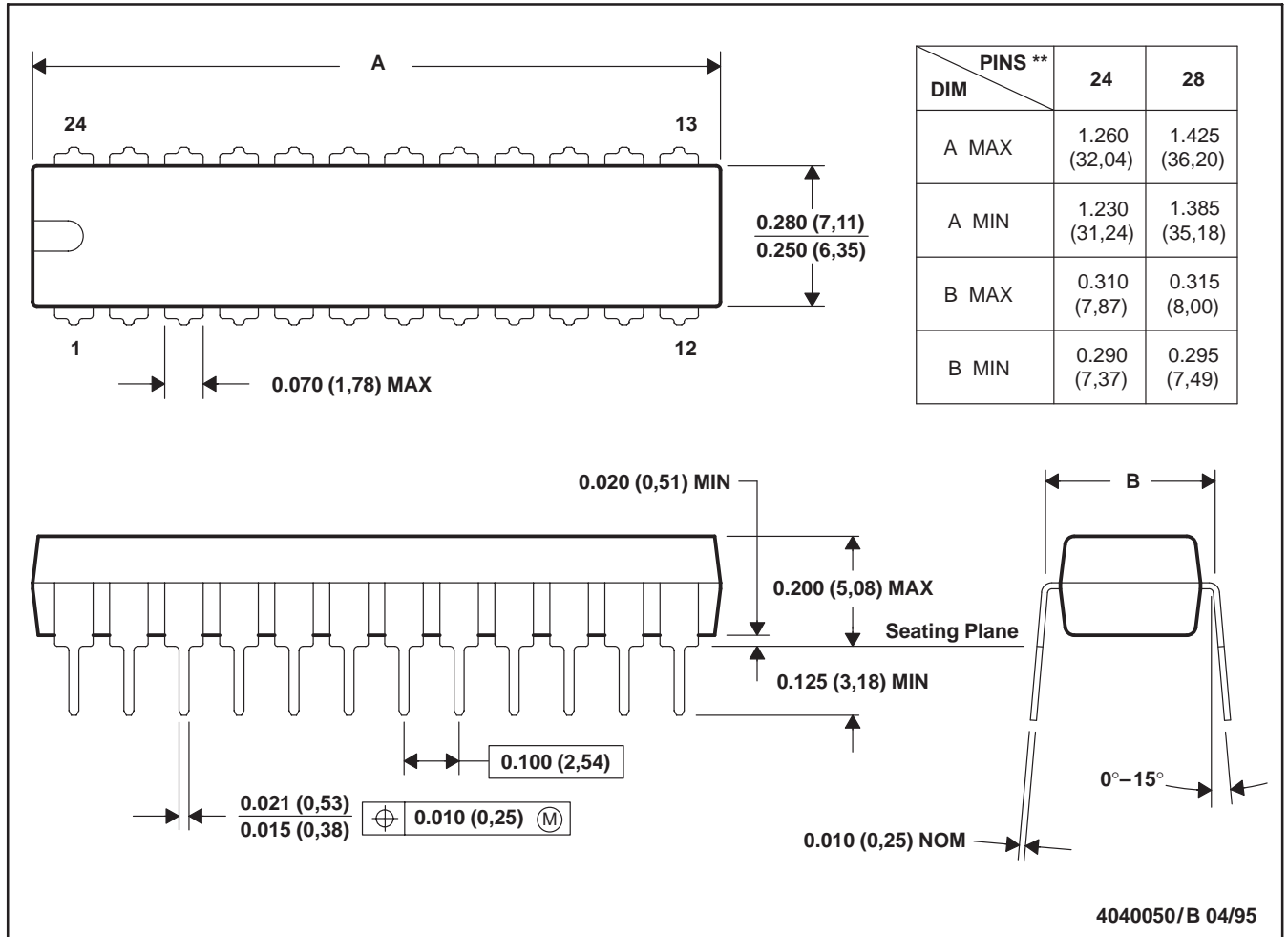
4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

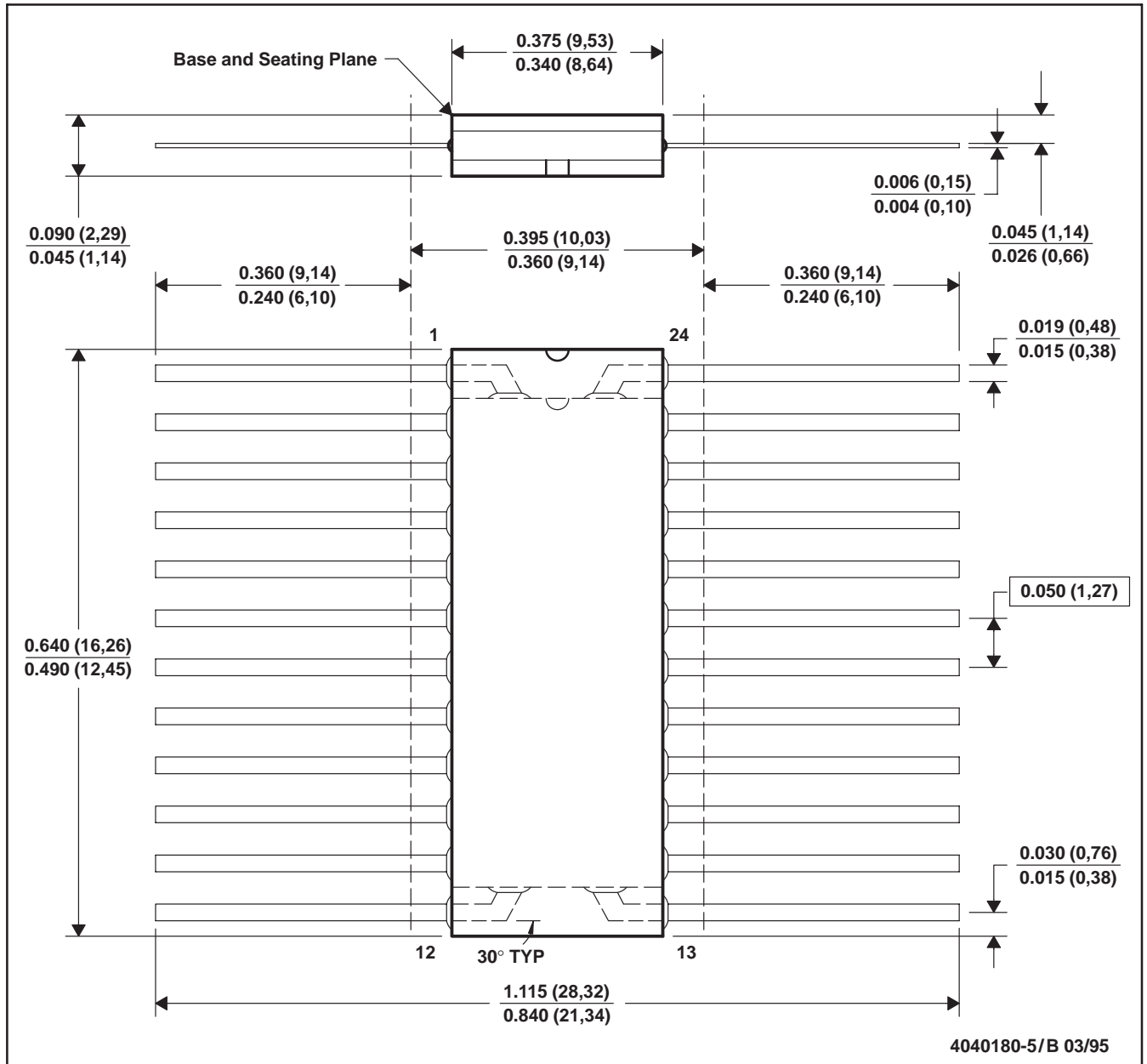
24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

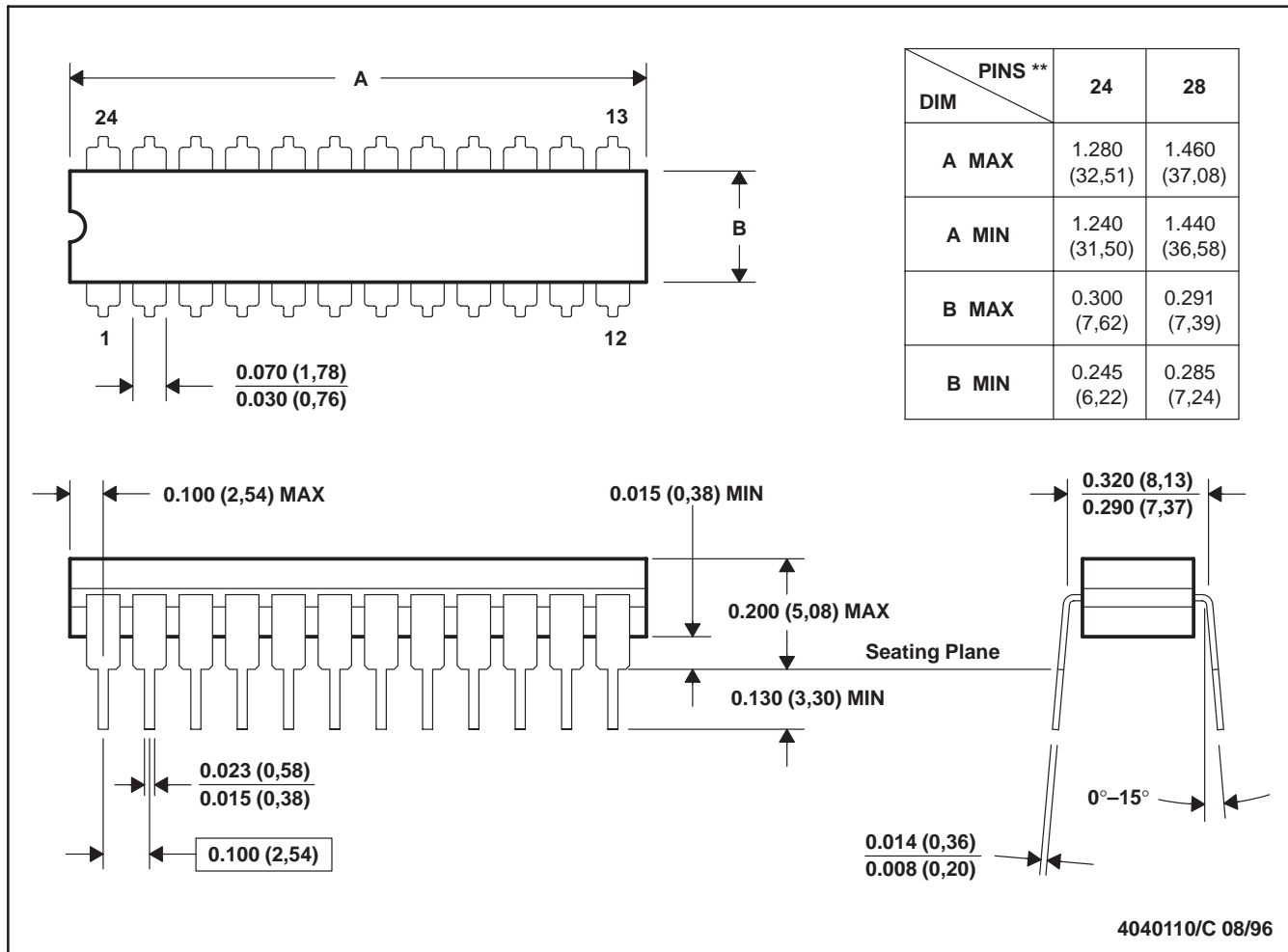


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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| Telephony | www.ti.com/telephony |
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| Wireless | www.ti.com/wireless |

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